WHAT IS CLAIMED IS:

1. A system for accelerating transmission control protocol (TCP) network traffic processing, the system comprising:

a network traffic reception module configured to receive TCP network traffic;

a hardware-based acceleration module configured to accelerate TCP network traffic processing in a steady state network connection, the acceleration module further configured with windowing functionality for performing flow control and congestion avoidance during TCP network traffic processing, and retransmission functionality for retransmitting packets in response to timeouts and errors as defined by a TCP network protocol; and

a software-based processing module configured to process TCP connection sequences, termination sequences, and non-steady state TCP network traffic.

2. The system of Claim 1 wherein, the hardware-based acceleration module is further configured to generate acknowledgement messages, manage flow control and congestion windows sizes, and handle re-transmission of messages according to the TCP network protocol.

3. The system of Claim 1 wherein the hardware-based acceleration module further comprises an accelerator sub-system that accelerates TCP protocol processing including congestion control, window management, acknowledgement, and retransmission policies associated with communications using the TCP protocol.

4. The system of Claim 3 further comprising a TCP control block (TCPCB) cache coupled with a prefetcher functionality associated with the accelerator sub-system to avoid stalls arising from memory transfers.

5. The system of Claim 4 wherein, the TCPCB cache and prefetcher functionality allow the hardware-based acceleration module to operate at approximately line rate.

6. The system of Claim 3 wherein, the accelerator sub-system utilizes a parallel register bus to transfer data into and out of register files in its components processors, thereby accelerating TCP protocol processing.

7. The system of Claim 3 wherein, the accelerator sub-system comprises a very long instruction word (VLIW) processor.

8. The system of Claim 7 wherein, the VLIW processor further comprises a plurality of arithmetic logic units (ALUs) and a shared register file that facilitate rapid processing of steady state network traffic.

9. The system of Claim 1 further comprising, an event machine module used to manage timers and accelerate timer processing associated with TCP protocol processing.

10. The system of Claim 1, wherein the hardware-based acceleration module implements a mutual exclusion mechanism to accelerate TCP protocol processing.

11. A system for accelerating network protocol processing, the system comprising:

a real-time acceleration module comprising a hardware-based network protocol processing component configured to accelerate network protocol processing in a steady state network connection performing functions including acknowledgement, windowing, and retransmission; and

a non-real-time module comprising a software-based module configured to process exception aspects of network protocol processing.

12. The system of Claim 11 wherein, the real-time and non-real-time modules are configured to operate with a plurality of networking protocols.

13. The system of Claim 11 wherein, the network protocol is represented by a TCP network protocol.

14. The system of Claim 11 wherein, the non-real-time module processes connection sequences, termination sequences, and non-steady state network traffic.

15. The system of Claim 11 wherein, the acknowledgement functionality of the real-time acceleration module comprises generating acknowledgment messages with appropriate parameters in response to incoming network packets.

16. The system of Claim 11 wherein, the windowing functionality of the real-time acceleration module comprises performing window management for flow control and congestion avoidance during network traffic processing.

17. The system of Claim 11 wherein, the retransmission functionality of the real-time acceleration module comprises retransmitting packets in response to timeouts and errors as defined by a selected network protocol.

18. The system of Claim 11 wherein, the acknowledgement, windowing, and retransmission functionalities of the real-time acceleration module include generating acknowledgement messages, managing flow control and congestion windows sizes, and handling re-transmission of messages.

19. The system of Claim 11 wherein the real-time acceleration module further comprises an accelerator sub-system that accelerates network protocol processing including congestion control, window management, acknowledgement, and retransmission policies associated with communication using a selected network protocol.

20. The system of Claim 19 wherein, the system is configured to process TCP network traffic and a TCP control block (TCPCB) cache is coupled with a prefetcher functionality associated with the accelerator sub-system to avoid stalls arising from memory transfers.

21. The system of Claim 20 wherein, the TCPCB cache and prefetcher functionality provide a means for the real-time acceleration module to operate at approximately line rate.

22. The system of Claim 19 wherein, the accelerator sub-system utilizes a parallel register bus to transfer data into and out of register files in its components processors, thereby accelerating network protocol processing.

23. The system of Claim 19 wherein, the accelerator sub-system comprises a very long instruction word (VLIW) processor.

24. The system of Claim 20 wherein, the VLIW processor further comprises a plurality of arithmetic logic units (ALUs) and a shared register file that facilitate rapid processing of steady state network traffic.

25. The system of Claim 11 wherein, the number of cycles used to complete protocol processing for each frame of steady state network traffic is between approximately 30-70 cycles.

26. The system of Claim 11 further comprising, an event machine module used to manage timers and accelerate timer processing associated with network protocol processing.

27. The system of Claim 11 wherein, the real-time acceleration module implements a hardware-based mutual exclusion mechanism to accelerate network protocol processing.

28. The system of Claim 11, wherein the real-time acceleration module is configured to perform network protocol processing in near real-time at near full line rate.

29. The system of Claim 11, wherein the non-real-time module is configured to perform network protocol processing at a rate less than the real-time acceleration module.

30. The system of Claim 11 wherein, the steady state network connection comprises a substantially uninterrupted period of in-sequence network packet reception.

31. The system of Claim 11 wherein, the steady state network connection comprises a substantially error free period of network packet reception.

32. The system of Claim 11 wherein, the steady state network connection comprises a period of packet reception wherein substantially no out-of-sequence network packets are received.